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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,355	10/06/2003	Bohumil Lojek	ATM-273	5650

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,355	LOJEK, BOHUMIL	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group I, specie II, claims 11-18 in the reply filed on 3/17/05 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-14, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Haver et al. (U.S. Patent No. 5,512,785).

Referring to figures 1-16, Haver et al. teaches a method of fabricating an electronic device comprising:

Forming a slot region (18) for a doped polycrystalline semiconductor plug material (28) within an outer periphery of an etched window region, the window region formed by etching a film stack (10/14) residing on a topmost surface of a substrate (see figure 6, col. 3, lines 12-43);

Filling the slot region with the polycrystalline semiconductor plug material (see figure 6, col. 3, lines 12-43), and

Depositing a dielectric separate layer (30, oxide) over the polycrystalline semiconductor plug and on an uppermost surface of the film stack (see col. 3, lines 22+, figure 7);

Depositing a spacer (34, see figure 8) over the dielectric separation layer;

Etching the spacer and the dielectric separation layer to form a dielectric boot shape () on a lower edge of the dielectric separation layer, the lower edge being portion of the dielectric separation layer proximal to the substrate (see figures 8-9, col. 3-4, lines 57-14); and

Redistributing a dopant from the polycrystalline semiconductor plug into the substrate (see figure 10, col. 4, lines 39-52).

Regarding to claim 12, the redistributing results in a doping concentration toroidal-like in topology (see figure 10).

Regarding to claim 13, implanting a dopant into an area of the substrate located in a region circumscribed by the slot region (see figure 10).

Regarding to claim 14, etching through any remaining film layers within a region substantially circumscribed by the dielectric boot to the topmost surface of the substrate (see figure 9, col. 4, lines 6-14) and depositing an emitter polycrystalline semiconductor layer (42, see figure 10, col. 4, lines 25-39) over the topmost surface of the substrate (see figure 10).

Regarding to claim 17, the spacer is comprised of polycrystalline silicon (34, figure 8, col. 3-4, lines 66-5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haver et al. (U.S. Patent No. 5,512,785) as applied to claims 11-14, 17 above in view of Zdebel et al. (U.S. Patent 5,026,663).

Haver et al. teaches forming an emitter base by depositing a stack film of oxide/poly/oxide/oxide/poly, forming a spacer of polycrystalline silicon, depositing a polysilicon plug. However, the reference does not teach the spacer is made of oxide (in claim 16), the film stack is comprised of a first oxide layer, a first nitride layer, a first polysilicon layer, a second nitride layer, and an isolation oxide (in claim 15), and filling the slot region with the polycrystalline semiconductor plug material is achieved by depositing a conformal polycrystalline semiconductor plug material and anisotropically etching the polycrystalline semiconductor plug material prior to depositing a dielectric separation layer (in claim 18).

Zdebel et al. forming an emitter base by forming the spacer is made of oxide (40/42), in claim 17), the film stack is comprised of a first oxide layer (14), a first nitride layer (16), a first polysilicon layer (18), a second nitride layer (22), and an isolation oxide (32, see col. 2-3, lines 45-27, in claim 15) and filling the slot region with the polycrystalline semiconductor plug material is achieved by depositing a conformal polycrystalline semiconductor plug material and

anisotropically etching the polycrystalline semiconductor plug material prior to depositing a dielectric separation layer (36, see col. 3, lines 45-56, figure 10-11, in claim 18).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form forming an emitter base by forming the spacer is made of oxide, the film stack is comprised of a first oxide layer, a first nitride layer, a first polysilicon layer, a second nitride layer, and an isolation oxide and filling the slot region with the polycrystalline semiconductor plug material is achieved by depositing a conformal polycrystalline semiconductor plug material and anisotropically etching the polycrystalline semiconductor plug material prior to depositing a dielectric separation layer in process of Haver et al. as taught by Zdebel et al. because the process would fabricate a structure having self-aligned diffused junctions that allows for semiconductor devices having increased speed, and the junction area precisely controlled and also allow for increased scalability and sub-micrometer dimensions as well as integrated contact through a horizontal semiconductor layer (see col. 1, lines 52+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800